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PATENT

I hereby certify that on the date specified below, this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

August 23, 2007

Date

A. Beggs

Alexandra Beggs

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Christophe J. Chevallier

Attorney Docket No.: 501111.01

Patent No. : US 6,944,812 B2

Issued : September 13, 2005

Title : MODE ENTRY CIRCUIT AND METHOD

Certificate

SEP 21 2007

of Correction

NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following errors were noted in a review of the above-identified letters patent. One or more of these errors was inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicant requests that this notification be placed in the Patent and Trademark Office file.

<u>Column, Line</u>	<u>Reads</u>	<u>Should Read</u>
Column 1, Line 13	"use different modes"	--use of different modes--
Column 1, Line 16	"that may found"	--that may be found--
Column 2, Line 52	"reference voltages power"	--reference voltage power--
Column 3, Line 49	"can be used during testing"	--to be used during testing--

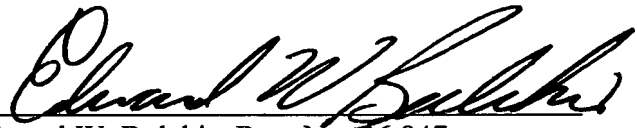
Column 5, Line 18	"between the an external"	--between an external--
Column 5, Line 22	"turn, executes the appropriate"	--turn executes the appropriate--
Column 5, Line 33	"I/O logic 412"	--I/O logic 412--
Column 7, Line 23	"voltage of the an input/output"	--voltage of the input/output
Column 8, Lines 5 and 30	"voltage of a input/output"	--voltage of an input/output--
Column 12, Line 34	"second reference voltages power supplies"	--second reference voltage power supplies--

Respectfully submitted,

Date:

Aug 21, 2007

By:



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Enclosure:

Postcard